Attorney Docket No.:ITEX-99001C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: *Liu et. al.*	)	Art Unit: *unknown*
Serial No.:*unknown*	)	
	)	Examiner: *unknown*
Filed: 11/13/01 as a continuation of serial no. 09/255,235 filed 2/22/99	)	
For: *DSL Link with Scaleable Performance*	)	

PRELIMINARY AMENDMENT

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Applicant respectfully submits the following amendment and response to place this case in condition for allowance:

IN THE SPECIFICATION:

Please change the title of the invention to read:

-- DSL Link with Scaleable Performance --

Please substitute the following for the Abstract:

<u>ABSTRACT OF THE DISCLOSURE</u>

A digital communications link, protocol and related circuits are disclosed which achieve a scaleable performance rate through a combination of clock scaling and/or variable frame sizing. The system is used within a personal computer, thus allowing the latter to be interoperable with any number of different communications protocols, including xDSL based transmission standards, and to set up communications links of varying capacity and performance.

Please delete the text at page 5, lines 5 – 17 and enter the following as a clean version substitute for such paragraph:

An improved digital communications link of the present invention connects a digital controller section of an xDSL modem - which is preferably located on a system motherboard of a computing system - to a separate analog section of the xDSL modem - which is located at a position substantially free of electronic noise from other electronic components on said motherboard, which could materially affect the operation of such analog section. The data path/link is generally configured in the following manner: (a) a plurality of receive signal lines are set up for receiving data from a remote site; (b) a plurality of transmit signal lines are designated for transmitting data to a remote site; (c) a bit clock signal line is set up for carrying a clock signal, which clock signal is used in connection with communicating the data to and from the remote site. The bit clock signal line can carry any desired clock signal needed according to data transmission requirements of said digital communications link, thus providing a scalable interface that is easily adaptable for use in any number of different motherboard environments.

Please enter the following as a clean version substitute for the paragraph in the specification at page 10, lines 1 – 11:

216, which transmits signals in the DSL link to DSL Digital Modem Circuit 230, and converts received signals in the DSL link to various data and control signals for the internal circuits within DSL Analog Modem Circuit 205, including control registers 215. Also inside DSL-A 216 is a clock circuit (not shown) which generates the necessary clocks for internal blocks and external DSL link based on an input from a System Master Clock as shown. Again, some or all of the functions of DSL Analog Modem Circuit 205 may be grouped and implemented in single chip form. For example, DSL-A codec 218, incorporating control registers 215, DSL-A Interface 216, digital filters 214, 214', and A/D 213 and D/A 213' is preferably embodied in a single integrated circuit (IC), and a separate IC is preferably used to embody analog front end sections (i.e. receive/transmit drivers 209, 209' and receive/transmit filters 211 and 211').

Please enter the following as a clean version substitute for the paragraph in the specification at page 11, lines 27 – 29:

As noted above, functions performed by Transmitter Buffer and Processing 234' and Receiver Buffer and Processing 234 depend on the specific xDSL implementation. In the case of host signal processing, where the present invention can be used for great

Please enter the following as a clean version substitute for the paragraph in the specification at page 12, lines 24 – 26:

Receive data lines RX_1 - RX_4 carry digital samples generated by A/D 213 and assembled and transmitted across the link by DSL-A Interface 216; DSL-D interface 233, conversely dis-assembles and passes these samples on for further signal processing.

Please enter the following as a clean version substitute for the paragraph in the specification at page 18, lines 11 – 29:

--Reuse of DSL Link for External Hardware DSL Implementation

As mentioned earlier, the use of DSL Link 220 is most attractive to a host based DSL modem implementation requiring minimal logic inside Digital IC 230. When the CPU in the motherboard is not fast enough, it is desirable to use the DSL Link to connect Digital IC 230 to an external hardware DSL implementation. In this case, another useful aspect of the present invention is illustrated in FIG. 4. As shown, when an external hardware solution for a DSL modem implementation exists, a reasonable interface to use with such implementation is one based on the ATM Utopia I or Utopia II interface. This is because ADSL technology has already been defined to interface with ATM in both T1.413 Issue 2 and ITU-T G.992 standards. In this configuration, DSL Digital IC 230 would be linked through DSL Digital Link 220 to a hardware based xDSL modem in FIG. 2A and 2B, instead of interfacing directly to DSL Analog Modem Circuit 205. In such instance, of course, since most of the signal processing and control functions would be located within the hardware xDSL modem, DSL Digital Controller 230 could be simplified accordingly. The reason this is possible is because the same 10 signal lines described above (RX_1 - RX_4, TX_1 - TX_4, CLOCK and WORD CLOCK) can serve a dual purpose and act as an ATM interface as well. As above, for the same four sampling cycles per word clock, the following data can be transported over DSL digital link 220:

1. First clock cycle period: RX_1 - RX_4 are used for Control, 0, RxClav, TxClav;

Please enter the following as a clean version substitute for the paragraph in the specification at page 19, lines 1 – 7:

TX_1 - TX_4 are used for Control, 0, RxEnb and TxEnb.

2. Second clock cycle period: RX_1 - RX_4 are used for RxSoc, RxAddr [2:0], while TX_1 - TX_4 are used for TxSoc, TxAddr [2:0].
3. Third clock cycle period: RX_1 - RX_4 are used for RxData [7:4], while TX_1 - TX_4 are used for TxData [7:4].
4. Fourth clock cycle period: RX_1 - RX_4 are used for RxData [3:0], while TX_1 - TX_4 are used for TxData [3:0].

IN THE CLAIMS:

Please cancel claims 17 – 31 and 37 - 60.

Please substitute the following as a clean set for remaining claims (1 – 16, 32 – 36 and 61 – 66):

1. (Amended) A method of implementing a digital communications link connecting a digital controller section of an xDSL modem, located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, said method comprising the steps of:

   (a) providing a plurality of receive signal lines for communicating data from a remote xDSL modem;

   (b) providing a plurality of transmit signal lines for communicating data to a remote xDSL modem;

   (c) providing a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal, which bit clock signal is generated by scaling a separate clock signal useable by the xDSL modem, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

2. (Amended) The method of claim 1, further including a step: providing a reset signal to reset the analog section of the xDSL modem.

3. (Original) The method of claim 1, wherein at least four (4) signal lines are used for said receive signal lines, and at least (4) separate signal lines are used for said transmit signal lines.

4. (Amended) The method of claim 1, further including a step of providing a word clock signal, which word clock signal has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining cycles being a second value.

5. (Original) The method of claim 1, wherein said receive and/or transmit signal lines can also be used for implementing an embedded operation channel within said receive and/or transmit signal lines, said embedded operation channel consisting of control signals embedded in both transmit and receive directions for use by the xDSL modem.

6. (Original) The method of claim 4, wherein at least one (1) bit per word clock cycle is used to carry control signals.

7. (Amended) The method of claim 5, wherein each control signal can have a first or a second length.

8. (Original) The method of claim 5, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and then idle bits are sent between control signals.

9. (Amended) The method of claim 1, further including a step: providing a multi-channel data frame during a plurality of consecutive bit clock periods based on said bit clock signal, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame, and further wherein said first and second time periods occur within said plurality of consecutive bit clock periods.

10. (Amended) The method of claim 9, wherein the number of channels in the multi-channel data frame is programmable.

11. (Amended) The method of claim 9, wherein said plurality of consecutive bit clock periods consists of at least four (4) bit clock cycles for each channel.

12. (Amended) The method of claim 11, wherein the boundary of each multi-channel data frame is indicated by a separate word clock signal having a first predetermined value at the frame beginning and a second predetermined value in the rest of the frame.

13. (Original) The method of claim 1, wherein said same receive and/or transmit signal lines can also be used to support a data interface between said digital controller and a hardware or DSP based xDSL modem.

14. (Original) The method of claim 13, wherein the data interface is logically equivalent to a Utopia I and/or II interface and said hardware or DSP based xDSL modem also can perform an ATM transport convergence (TC) function.

15. (Original) The method of 14, wherein an embedded operation channel (EOC) is used to control proper operations of the hardware or DSP based xDSL modem.

16. (Amended) The method of claim 1, wherein said separate clock signal is based on a master clock external to the xDSL modem and operated at a frequency required by the digital communications link.

32. (Amended) A method of implementing a digital communications link within a personal computer system, comprising the steps of:

(a) providing a plurality of receive signal lines, said receive signal lines being configurable such that data can be received by a digital controller from both an analog codec and an ATM interface;

(b) providing a plurality of transmit signal lines, said transmit signal lines being configurable such that data can be transmitted by a digital controller to both an analog codec and an ATM interface;

(c) providing a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with both an analog codec and an ATM interface;

(d) providing a data transfer protocol such that data transfers over said digital communications link can include codec samples and/or ATM cell data;

wherein said bit clock further can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link.

33. (Original) The method of claim 32, wherein said ATM interface is logically equivalent to an ATM Utopia I and II interfaces.

34. (Amended) The method of claim 32, wherein the digital controller is located on a system motherboard of the personal computer system, and said analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog codec.

35. (Amended) The method of claim 32, wherein said digital communications link supports a plurality of data channels by time division multiplexing data transfers using a frame signal related to said clock signal.

36. (Amended) The method of claim 32, wherein operational and/or control information for said analog codec and/or can be embedded in data frames communicated through the plurality of receive and transmit signal lines.

61. (Amended) In a motherboard for use in a personal computing system, and which system is configured to treat a high speed xDSL capable modem as a motherboard device, the improvement comprising:

(A) a digital controller associated with the high speed modem, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing xDSL formatted data and control signals; and

(B) an analog front end circuit associated with the high speed modem, said analog front end circuit being electrically coupled but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a clock signal adapted for an xDSL compatible link, said clock signal being generated by scaling a separate clock signal useable by the xDSL capable modem, such that said clock signal is variable to accommodate a plurality of different xDSL transmission protocols; and

wherein said digital interface supports an xDSL compatible data link between said digital controller and said analog front end circuit.

62. (Original) The motherboard of claim 61, wherein said analog front end circuit is located on a riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. (Original) The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. (Original) The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

65. (Amended) The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be used to support an Asynchronous Transfer Mode (ATM) interface.

66. (Amended) The motherboard of claim 65, wherein said ATM interface is a Utopia I and/or II interface.

Please add new claims 67 – 120:

67. (New) A method of transmitting data over an xDSL digital communications link between a digital controller portion of an xDSL modem and an analog codec portion of the xDSL modem, comprising the steps of:

(a) selecting an xDSL transmission protocol to be used in the xDSL digital communications link; and

(b) configuring a bit clock to accommodate transmission requirements of said selected xDSL transmission protocol, said bit clock being generated by scaling a separate clock signal useable by the xDSL modem; and

(c) communicating data between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link using said bit clock; and

wherein said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

68. (New) The method of claim 67, wherein said separate clock signal is a master clock signal used by the xDSL modem, and said bit clock is derived by dividing said master clock signal by a value specified for said xDSL transmission protocol.

69. (New) The method of claim 68, wherein said value specified for said xDSL transmission protocol is programmed and stored in a register of the analog codec portion of the xDSL modem.

70. (New) The method of claim 67, wherein the xDSL digital communications link is embodied as a bus located on a motherboard of a personal computer system.

71. (New) The method of claim 67, wherein said bit clock is used for both receive and transmit data.

72. (New) The method of claim 67, further including a step: (d) generating a word clock based on said bit clock for communicating data words between the digital controller portion of the xDSL modem and the analog codec portion of the xDSL modem across the xDSL digital communications link, said word clock having a period equal to a plurality of bit clock periods.

73. (New) The method of claim 67, further including a step: (d): transmitting a frame of data across the xDSL digital communications link, said frame of data occupying a plurality of consecutive bit clocks.

74. (New) The method of claim 73, wherein said frame of data is transmitted by dividing it over multiple communications lines.

75. (New) The method of claim 73, wherein said frame of data is signalled by a word clock being held in an active state for more than one bit clock period.

76. (New) The method of claim 67, wherein said xDSL transmission protocols include Asymmetric Digital Subscriber Loop (ADSL) protocols.

77. (New) The method of claim 67, wherein said data includes digital samples generated by an analog to digital converted forming part of the analog codec portion of the xDSL modem, and said digital samples are processed by host signal processing circuitry to support the xDSL modem.

78. (New) The method of claim 67, wherein said host signal processing circuitry includes a FFT circuit embedded in a digital controller as well as software executing on a host processor.

79. (New) The method of claim 67, wherein said data includes Asynchronous Transfer Mode (ATM) based data cells, and said ATM based data cells are processed by a hardware based signal processor to support the xDSL modem.

80. (New) The method of claim 67, wherein steps (a), (b) and (c) are performed by the digital controller portion of the xDSL modem incorporated as part of a North Bridge and/or a South Bridge chipset.

81. (New) The method of claim 67, wherein step (c) is performed by the analog codec portion of the xDSL modem which is located on a separate board from the digital controller.

82. (New) The method of claim 67, wherein said bit clock can have a frequency exceeding 35 Mhz.

83. (New) A system for implementing a digital communications link connecting a digital controller section of an xDSL modem located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be substantially free of electronic noise from other electronic components on the motherboard which could significantly affect the overall operation of such xDSL modem, the system comprising:

(a) plurality of receive signal lines implemented as part of a communications bus within the computing system for communicating data from a remote xDSL modem;

(b) a plurality of transmit signal lines implemented as part of said communications bus for communicating data to a remote xDSL modem;

(c) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal to clock transfers for said communications bus;

wherein said bit clock signal has a variable frequency that can be set to accommodate a plurality of different xDSL transmission protocols.

84. (New) The system of claim 83, wherein said bit clock can have a frequency exceeding 35 Mhz.

85. (New) The system of claim 83, wherein said bit clock signal is generated by the digital controller section integrated in a North Bridge or South Bridge chipset.

86. (New) The method of claim 83, wherein said bit clock signal is generated by the separate analog section of the xDSL modem on a modem riser card.

87. (New) The system of claim 83, wherein the system is incorporated within a North Bridge and/or a South Bridge chipset.

88. (New) The system of claim 83, wherein the system is incorporated within a motherboard for a computer system.

89. (New) The system of claim 83, further including an interface for transferring data over a USB based bus.

90. (New) The system of claim 89, further including an interface for transferring data over an AC – 97 based bus.

91. (New) The system of claim 90, further including an interface for transferring data over a PCI bus.

92. (New) A communications protocol for transmitting data over a digital communications link within a computer system between a digital controller and an analog coder/decoder (CODEC), the protocol comprising the steps of:

(a) generating a bit clock adapted for data transmission requirements of the digital communications link;

(b) generating a separate frame signal for indicating a boundary for a variable sized data frame transmitting the data between the digital controller and the analog CODEC;

(c) supporting a scaleable data rate in the digital communications link by adjusting a clock rate of said bit clock and/or a size of said variable sized data frame.

93. (New) The communications protocol of claim 92 wherein said clock rate is varied in accordance with an xDSL transmission standard used in the digital communications link.

94. (New) The communications protocol of claim 92 wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

95. (New) The communications protocol of claim 94 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

96. (New) The communications protocol of claim 94 wherein said number of active data channels is programmed by the digital controller.

97. (New) The communications protocol of claim 94 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog codecs.

98. (New) The communications protocol of claim 92 wherein said frame signal is based on a word clock signal, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

99. (New) An input/output (I/O) circuit for supporting a communications link over a computer bus used within a computer system between a digital controller and an analog coder/decoder (CODEC), the I/O circuit including:

a digital communications interface including:

1) a plurality of receive lines for receiving data; and

2) a plurality of transmit lines, separate from said plurality of receiving lines, for transmitting data;

wherein the data is transferred in parallel across said plurality of receive lines and said plurality of transmit lines in accordance with the bus protocol;

3) a bit clock signal line, separate from said plurality of receive signal lines and said plurality of transmit signal lines, for carrying a bit clock signal adapted for a transmission protocol supported by the bus protocol;

4) a frame clock signal line for carrying a frame clock signal adapted for clocking a variable sized data frame in accordance with the bus protocol, said variable sized data frame having a size based on a number of active channels in the plurality of separate data channels and/or a desired data rate;

wherein said plurality of receive lines, said plurality of transmit lines, said bit clock signal line and said frame clock signal line support the bus protocol as part of the communications bus within the personal computer system.

100. (New) The I/O circuit of claim 99 wherein said clock rate is varied in accordance with an xDSL transmission standard used in the digital communications link.

101. (New) The I/O circuit of claim 99 wherein said size of said variable sized data frame is adjusted by changing a number of active data channels used in the digital communications link.

102. (New) The I/O circuit of claim 101 wherein said number of active data channels can be varied in both a transmit and receive direction in the digital communications link.

103. (New) The I/O circuit of claim 101 wherein said number of active data channels is programmed by the digital controller.

104. (New) The I/O circuit of claim 101 wherein said number of active data channels is used to support a plurality of separate communication links with a plurality of respective separate analog CODECs.

105. (New) The I/O circuit of claim 99 wherein said frame signal is based on a word clock signal generated by the digital interface, said word clock signal being used for clocking a sample data word from an analog to digital (A/D) converter in the CODEC.

106. (New) A method of communicating data between a first integrated circuit located on a computer motherboard and a second integrated circuit located on the computer motherboard, the method comprising the steps of:

(a) communicating transmit data from the first integrated circuit to the second integrated circuit using a plurality of data transmit signal lines for; and

(b) communicating receive data from the second integrated circuit to the first integrated circuit using a plurality of data receive signal lines, wherein said data receive signal lines are separate from said data transmit signal lines; and

wherein both transmit and receive data can be communicated at the same time between said first integrated circuit and said second integrated circuit over said plurality of data transmit signal lines and said plurality of data receive signal lines;

(c) providing a first clock signal on a first clock signal line, said first clock signal being adjustable based on a transmit transfer rate to be used for said transmit data; and

(d) providing a second clock signal on a second clock signal line, said second clock signal being adjustable based on a receive transfer rate to be used for said receive data;

wherein both said transmit transfer rate and said receive transfer rate can be independently configured for data communications between the first integrated circuit and the second integrated circuit.

107. (New) The method of claim 106 wherein a transmit data word is clocked in parallel over said plurality of data transmit signal lines, such that a first portion of said data word is transferred over a first data transmit signal line of said plurality of data transmit signal lines, and a successive second portion of said data word is transferred over a separate second data transmit signal line of said plurality of data transmit signal lines.

108. (New) The method of claim 106 where said first portion is a bit, and said first clock signal is a bit clock.

109. (New) The method of claim 106 wherein both a scaleable transmit transfer rate and a scaleable receive transfer rate can be generated based on a value set in a control register within the second integrated circuit.

110. (New) The method of claim 106 wherein the first integrated circuit and second integrated circuit are coupled by an asymmetric communications link in which said transmit transfer rate and said receive transfer rate differ substantially from each other.

111. (New) The method of claim 106 wherein said transmit transfer rate and/or said receive transfer rate are also configurable by adjusting a number of time slots used within a transmit frame and/or a receive frame communicated between the first integrated circuit and the second integrated circuit.

112. (New) The method of claim 111 wherein said transmit frame and/or said receive frame can be configured to set up multiple communications channels between the first integrated circuit and a plurality of second integrated circuits.

113. (New) A method of communicating data over a data link connecting a first integrated circuit located on a computer motherboard and a second integrated circuit located on the computer motherboard, the method comprising the steps of:

(a) communicating first transmit data from the first integrated circuit to the second integrated circuit over the data link using a first transmission channel; and

(b) communicating first receive data from the second integrated circuit to the first integrated circuit over the data link using a first receive channel, said first receive channel and said first transmission channel being separate; and

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a scaleable clock signal;

wherein said scaleable clock signal is adjusted for the data link between the first integrated circuit and the second integrated circuit so that the data link uses a scaleable clock rate to support a data transfer rate required for said first transmission channel and/or said first receive channel.

114. (New) The method of claim 113 further including a step of setting up a second transmission channel and a second receive channel over the data link between the first integrated circuit and a third integrated circuit to support second transmit data and second receive data respectively using said scaleable clock signal.

115. (New) The method of claim 113 wherein said scaleable clock rate is used to generate a transmit clock rate used in said first transmission channel and a separate receive clock rate used in said first receive channel, such that said transmit clock rate and said separate receive clock rate are related by an integer ratio.

116. (New) The method of claim 115 wherein said integer ratio is provided in a control register in the second integrated circuit.

117. (New) The method of claim 113 wherein said scaleable clock signal is a bit clock used in both said first transmit channel and said first receive channel.

118. (New) The method of claim 113 wherein said data link is set up over a computer bus located on the computer motherboard.

119. (New) The method of claim 113 further including a step of providing a data word clock for effectuating said data transmissions in the form of data words transferred over the data link, said data words including a fixed number of data bits such that said data word clock has a period corresponding to multiple scaleable clock signals.

120. (New) The method of claim 113 further including a step: time division multiplexing control information and data over said first transmission channel so as to provide control information from the first integrated circuit to said second integrated circuit as part of said data transmission, said control information including a power management signal including at least a wake-up signal and/or a power down signal.

Remarks

Claims 1 – 16, 32 – 36 and 61 – 120 are pending. The present application is a continuation of parent application serial no. 09/255,235, which is now allowed.

The present claims are more particularly directed to those aspects of the invention that relate to communications links within a computer system that allow flexible scaleability and performance. This includes the use of a scaleable clock signal to accommodate a plurality of different transmission protocols, including in particular, various xDSL related standards (i.e., g.lite, g.dmt, T1.413, VDSL, HDSL, SDSL, ADSL, etc.). The scaleable clock signal is preferably a bit clock signal generated by scaling a separate clock signal, which in some cases can be an external system clock, or even an internally generated communications clock. *See, e.g.,* claims 1 – 16, 32 – 36 and 61 - 91. Support for this aspect of the invention can be found at among other places, pages 13 – 15. In this fashion, unlike the prior art that uses only a fixed clock rate, the system can enable an internal xDSL modem to be interoperable and self-configuring with any number of different communications transmission requirements. New claims 106 – 112 are further directed to specific embodiments where two separate adjustable clock signals can be used for receive/transmit channels, while new claims 113 – 120 are directed to embodiments where both receive/transmit channels use a scaleable clock signal. These features are advantageous, for example, where asymmetric data rates are used in the link between a receive and transmit channel. *See* pages 13 – 17.

New claims 92 – 105 are similarly directed to scaleable performance features that arise as a result of changing the size of a variable sized data frame. Again, this is quite different from prior art techniques (such as AC – 97 communications links), in which, for example, only a fixed number of time slots could be allocated for any particular channel, and the overall number of slots is also constant. This feature of the invention is further explained in the specification at pages 16 – 18.

Conclusion

For the reasons set forth above, Applicants submit that the pending claims should be allowable.

A fee transmittal sheet is enclosed; please charge any additional filing fees for the extra claims submitted herewith to deposit account no. 501-244.

Respectfully submitted,

J. Nicholas Gross
Registration No. 34,175
Attorney for Applicants

November 13, 2001
1385 Mission Street
Suite 240
San Francisco, CA 94103
(415) 551 - 8298

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 13th day of November, 2001.

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE SPECIFICATION

Page 5, ll. 5 – 17:

An improved digital communications link of the present invention connects a digital controller section of an xDSL modem - which is preferably located on a system motherboard of a computing system - to a separate analog section of the xDSL modem - which is located at a position substantially free of electronic noise from other electronic components on said motherboard, which could materially affect the operation of such analog section. The data path/link is generally configured in the following manner: (a) a plurality of receive signal lines are set up for receiving data from a remote site; (b) a plurality of transmit signal lines are designated for transmitting [receiving] data to [from] a remote site; (c) a bit clock signal line is set up for carrying a clock signal, which clock signal is used in connection with communicating the data to and from the remote site. The bit clock signal line can carry any desired clock signal needed according to data transmission requirements of said digital communications link, thus providing a scalable interface that is easily adaptable for use in any number of different motherboard environments.

Page 10, lines 1 – 11:

216, which transmits signals in the DSL link to DSL Digital Modem Circuit 230, and converts received signals in the DSL link to various data and control signals for the internal circuits within DSL Analog Modem Circuit 205, including control registers 215. Also inside DSL-A 216 [218] is a clock circuit (not shown) which generates the necessary clocks for internal blocks and external DSL link based on an input from a System Master Clock as shown. Again, some or all of the functions of DSL Analog Modem Circuit 205 may be grouped and implemented in single chip form. For example, DSL-A codec 218, incorporating control registers 215, DSL-A Interface 216, digital filters 214, 214', and A/D 213 and D/A 213' is preferably embodied in a single integrated circuit (IC), and a separate IC is preferably used to embody analog front end sections (i.e. receive/transmit drivers 209, 209' and receive/transmit filters 211 and 211').

Page 11, lines 27 – 29:

As noted above, functions performed by Transmitter Buffer and Processing 234' [234] and Receiver Buffer and Processing 234 [234'] depend on the specific xDSL implementation. In the case of host signal processing, where the present invention can be used for great

Page 12, lines 24 – 26:

Receive data lines RX_1 - RX_4 carry digital samples generated by A/D 213 and assembled and transmitted across the link by DSL-A Interface 216; DSL-D interface 233, conversely dis-assembles and passes these samples on for further signal processing.

Page 18, lines 11 – 29:

--Reuse of DSL Link for External Hardware DSL Implementation

As mentioned earlier, the use of DSL Link 200 [220] is most attractive to a host based DSL modem implementation requiring minimal logic inside Digital IC 230. When the CPU in the motherboard is not fast enough, it is desirable to use the DSL Link to connect Digital IC 230 to an external hardware DSL implementation. In this case, another useful aspect of the present invention is illustrated in FIG. 4. As shown, when an external hardware solution for a DSL modem implementation exists, a reasonable interface to use with such implementation is one based on the ATM Utopia I or Utopia II interface. This is because ADSL technology has already been defined to interface with ATM in both T1.413 Issue 2 and ITU-T G.992 standards. In this configuration, DSL Digital IC 230 would be linked through DSL Digital Link 220 to a hardware based xDSL modem in FIG. 2A and 2B, instead of interfacing directly to DSL Analog Modem Circuit 205. In such instance, of course, since most of the signal processing and control functions would be located within the hardware xDSL modem, DSL Digital Controller 230 could be simplified accordingly. The reason this is possible is because the same 10 signal lines described above (RX_1 - RX_4, TX_1 - TX_4, CLOCK and WORD CLOCK) can serve a dual purpose and act as an ATM interface as well. As above, for the same four sampling cycles per word clock, the following data can be transported over DSL digital link 220:

1. First clock cycle period: RX_1 - RX_4 are used for Control, 0, RxClav, TxClav;

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TX_1 - TX_4 are used for Control, 0, RxEnb and TxEnb.

2. Second clock cycle period: RX_1 - RX_4 are used for RxSoc, RxAddr [2:0], while TX_1 - TX_4 are used for TxSoc, TxAddr [2:0].

3. Third clock cycle period: RX_1 - RX_4 are used for RxData [7:4] ~~[3:0]~~, while TX_1 - TX_4 are used for TxData [7:4] ~~[3:0]~~.

4. Fourth clock cycle period: RX_1 - RX_4 are used for RxData [3:0] ~~[4:7]~~, while TX_1 - TX_4 are used for TxData [3:0] ~~[4:7]~~.

VERSION WITH MARKINGS TO SHOW CHANGES TO CLAIMS

1. (Amended) A method of implementing a digital communications link connecting a digital controller section of an xDSL modem, located on a system motherboard of a computing system, to a separate analog section of the xDSL modem adapted to be [, located at a position which is] substantially free of electronic noise from other electronic components on [said] the motherboard which could significantly affect the overall operation of such [said] xDSL modem, said method comprising the steps of:

   (d) providing a plurality of receive signal lines for communicating data from a remote xDSL modem;

   (e) providing a plurality of transmit signal lines for communicating data to a remote xDSL modem;

   (f) providing a bit clock signal line separate from said plurality of receive signal lines and said plurality of transmit signal lines for carrying a bit clock signal, which bit clock signal is [used in connection with communicating said data to and from said remote xDSL modem; said bit clock being] generated by scaling a separate clock signal useable by the xDSL modem, such that said bit clock is variable to accommodate a plurality of different xDSL transmission protocols.

   [(d) providing a word clock signal to mark the boundary for a sample word received or transmitted on said plurality of receive signal lines and plurality of transmit signal lines.]

2. (Amended) The method of claim 1, further including a step [(e)]: providing a reset signal to reset the analog section of the xDSL modem.

3. (Original) The method of claim 1, wherein at least four (4) signal lines are used for said receive signal lines, and at least (4) separate signal lines are used for said transmit signal lines.

4. (Amended) The method of claim 1, further including a step of providing a word clock signal, which [wherein the] word clock signal has a cycle consisting of at least four (4) bit clock cycles, with the first cycle being a first value and the remaining cycles being a second value.

VERSION WITH MARKINGS TO SHOW CHANGES TO CLAIMS

5. (Original) The method of claim 1, wherein said receive and/or transmit signal lines can also be used for implementing an embedded operation channel within said receive and/or transmit signal lines, said embedded operation channel consisting of control signals embedded in both transmit and receive directions for use by the xDSL modem.
6. (Original) The method of claim 4, wherein at least one (1) bit per word clock cycle is used to carry control signals.
7. (Amended) The method of claim 5, wherein each control signal can have [either] a first or a second length.
8. (Original) The method of claim 5, wherein each control signal begins with a start bit, is followed by a length bit, then by a set of command bits, and then idle bits are sent between control signals.
9. (Amended) The method of claim 1, further including a step: providing a multi-channel data frame during a plurality of consecutive bit clock periods based on said bit clock signal, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame, and further wherein said first and second time periods occur within said plurality of consecutive bit clock periods.
10. (Amended) The method of claim 9, wherein the number of channels in the multi-channel data frame is programmable.
11. (Amended) The method of claim 9, wherein [the word clock] said plurality of consecutive bit clock periods consists of at least four (4) bit clock cycles for each channel.
12. (Amended) The method of claim 11, wherein [said same word clock signal is used to mark] the boundary of each multi-channel data frame is indicated by a separate word clock signal having a first predetermined value [for two bit clock cycles] at the frame beginning and [said word clock signal has said] a second predetermined value [for only one bit clock cycle for each word beginning] in the rest of the frame.
13. (Original) The method of claim 1, wherein said same receive and/or transmit signal lines can also be used to support a data interface between said digital controller and a hardware or DSP based xDSL modem.

VERSION WITH MARKINGS TO SHOW CHANGES TO CLAIMS

14. (Original) The method of claim 13, wherein the data interface is logically equivalent to a Utopia I and/or II interface and said hardware or DSP based xDSL modem also can perform an ATM transport convergence (TC) function.
15. (Original) The method of 14, wherein an embedded operation channel (EOC) is used to control proper operations of the hardware or DSP based xDSL modem.
16. (Amended) The method of claim 1, wherein said [bit] <u>separate</u> clock signal is based <u>on a</u> [an external] master clock <u>external to the xDSL modem and</u> operated at a frequency required by [said xDSL modem] <u>the digital communications link</u>.

VERSION WITH MARKINGS TO SHOW CHANGES TO CLAIMS

32. (Amended) A method of implementing a digital communications link within a personal computer system, comprising the steps of:

(a) providing a plurality of receive signal lines, said receive signal lines being configurable such that data can be received by a digital controller from both an analog codec [and/or a hardware or DSP based xDSL modem with] and an ATM interface;

(b) providing a plurality of transmit signal lines, said transmit signal lines being configurable such that data can be transmitted by a digital controller to both an analog codec [and/or a hardware or DSP based xDSL modem with] and an ATM interface;

(c) providing a clock signal line, said clock signal line carrying a clock signal adapted for data transfers associated with both an analog codec [and/or a hardware or DSP based xDSL modem with] and an ATM interface;

(d) providing a data transfer protocol such that data transfers over said digital communications link can include [conventional xDSL] codec samples and/or ATM cell data; wherein said bit clock further can be varied to accommodate a plurality of different data transfer protocols used in the digital communications link.

33. (Original) The method of claim 32, wherein said ATM interface is logically equivalent to an ATM Utopia I and II interfaces.

34. (Amended) The method of claim [33] 32, wherein the digital controller [section] is located on a system motherboard of the personal computer system, and [the]said analog codec is located at a position which is substantially free of electronic noise from other electronic components on said motherboard which could materially affect the operation of such analog [CODEC] codec.

35. (Amended) The method of claim 32, wherein said digital communications link supports a plurality of data channels by time division multiplexing data transfers using a [word clock] frame signal related to said clock signal.

36. (Amended) The method of claim 32, wherein operational and/or control information for said analog codec and/or [hardware/DSP based xDSL modem] can be embedded in data [words] frames communicated through the plurality of receive and transmit signal lines.

61. (Amended) In a motherboard for use in a personal computing system, and which system is configured to treat a high speed xDSL capable modem as a motherboard device, the improvement comprising:

(A) a digital controller associated with the high speed modem, said digital controller being located physically on the motherboard and including:

[i] circuitry for processing xDSL formatted data and control signals; and

(B) an analog front end circuit associated with the high speed modem, said analog front end circuit being electrically coupled but physically separated from said digital controller, said analog front end circuit including:

[i] line interface circuitry for coupling to a data channel carrying analog data signals corresponding to said xDSL formatted data and control signals; and

[ii] circuitry for performing A/D and D/A operations on said analog data signals and xDSL formatted data and control signals respectively; and

(C) a digital interface for coupling said digital controller and analog front end circuit, said digital interface including:

[i] a plurality of xDSL data receiving lines; and

[ii]a plurality of xDSL data transmitting lines; and

[iii] a clock signal adapted for an xDSL compatible link, said clock signal being generated by scaling a separate clock signal useable by the xDSL capable modem, such that said clock signal is variable to accommodate a plurality of different xDSL transmission protocols; and

[[iv] an embedded control channel data in said xDSL compatible link;]

wherein said digital interface supports an xDSL compatible data link between said digital controller and said analog front end circuit.

62. (Original) The motherboard of claim 61, wherein said analog front end circuit is located on a riser card which is configured to be mounted substantially perpendicular to the motherboard.

63. (Original) The motherboard of claim 61, wherein said digital controller is controlled in part in software by a host processor located on the motherboard.

64. (Original) The motherboard of claim 61, further wherein said digital interface uses a multi-channel data frame, said multi-channel data frame having at least two data channels, and wherein data is transferred through a first channel during a first time period of said multi-channel data frame, and through a second channel during a second time period of said multi-channel data frame.

65. (Amended) The motherboard of claim 61, wherein said receive and/or transmit signal lines can also be used to support an Asynchronous Transfer Mode (ATM) [ATM] interface [for a hardware based xDSL modem].

66. (Amended) The motherboard of claim [61] 65, wherein said ATM interface is a Utopia I and/or II interface.